IN THE SPECIFICATION

Please amend the Title on page 1 as follows:

~~SEMICONDUCTOR DEVICE~~ INJECTION ENHANCED GATE TRANSISTOR INCLUDING SECOND EMITTER IN DUMMY REGION TO PREVENT WAVEFORM VIBRATION ASSOCIATED WITH NEGATIVE GATE CAPACITANCE

Please amend the paragraph at page 1, lines 16-22 as follows:

In the field of power semiconductor devices, there is a strong request for low on-voltage and reduction of turn-off loss in addition to enhancement of resistance to high breakdown voltage and availability for larger current. To meet these requirements, IEGT (~~Injected~~ Injection Enhanced Gate Transistor) has been developed as a further improvement of IGBT (Insulated Gate Bipolar Transistor).

Please amend the paragraph at page 12, lines 10-18 as follows:

On the other hand, the range of V_{ge} in the instant embodiment belongs to NCR1 and NCR2 where R_{float} is equal to or lower than 3Ω, and these ranges are positioned above $V_{ge\ (on)}$. In this case, since V_{ge} takes the turn-on state before affected by the negative capacitance, overshoot of V_{ge} is prevented, and dV/dt is controlled in an appropriate value. The aforementioned relation between R_{float} and $V_{ge\ (on)}$ has been described in U.S. patent application No.~~10,354,048~~ 10/354,048, the contents of which are incorporated herein by reference.

Please amend the paragraph at page 14, lines 12-26 as follows:

The IEGT 6 shown in Fig. 10 is formed on a SOI (silicon-on-insulator) substrate having a semiconductor support layer 64, insulating layer [[62]] 12 and a semiconductor active layer 60. The active layer 60 is used as a high-resistance n-type drift layer (n-type base

layer) 10. On a right portion of Fig. 10, a p-type collector layer 66 and a collector electrode 68 are located. In a region of a left portion of Fig. 10, which is remote from the p-type collector layer 66, a p-type base layer is formed on the n-type drift layer 10, and trenches TR are formed from the top surface of the p-type base layer. Thus, the p-type base layer is divided to the first base layer 16 of the main cell region MC and the second base layer 18 of the dummy cell region DC. Around the trenches TR, the same structure as the upper part of the IEGT 1 of Fig. 2 is formed.

Please amend the paragraph at page 14, line 27 through page 15, line 3 as follows:

In the IEGT 1 shown in Fig. 2, having the vertical structure in which the collector electrode 26 and the emitter electrode 28 are formed to sandwich the substrate, the main current flows vertically through the n-type drift layer 10. In contrast, in the IEGT 6 shown in Fig. [[11]] 10, having the lateral type structure in which the collector electrode 68 and the emitter electrode 28 are located on a common side of the substrate, the main current flows laterally in the n-type drift layer 10. In the other respects, however, both these types of devices work under identical operational principles. As such, the present invention is applicable not only to vertical type IEGTs but also to lateral type IEGTs.